25. (Amended) A semiconductor device according to Claim 2,

wherein said plurality of first MOS transistors are p-channel type, and the source of each of said plurality of first MOS transistors is supplied with said first voltage, and

wherein said plurality of second MOS transistors are p-channel type, and the source of each of said plurality of second MOS transistors is supplied with said second voltage.

Please cancel Claim 26 without prejudice.

REMARKS

Favorable reconsideration of this application, as amended, is respectfully requested.

Claims 1-7 and 21-25 have been amended to clarify th invention intended to be claimed. The rejection under 35 U.S.C. § 112 has been overcome by avoiding the phrase "minimum processing dimension".

The rejection under 35 U.S.C. § 103(a) is respectfully traversed, particularly insofar as that rejection might be considered applicable to Claims 1-7 and 21-25 now presented. Claim 26 has been cancelled as no longer necessary.

Although the rejection states that Claims 1-7 and 21-26 are unpatentable over Fifield et al. (page 4 of the Office Action), the body of the rejection on pages 5 and 6 of the Office Action refers to "Fang" or "Feng" (presumably U.S. Patent No. 6,417,037) listed on PTO-892.

Independent Claim 1 now recites, inter alia, a gate length of a first gate electrode of a plurality of first MOS transistors that is larger than a gate length of a second gate electrode of a plurality of second MOS transistors, and a spacing between the first gate electrod of the first MOS transistors and the first contact hole for connecting a wiring to a source region or a drain region of the first MOS transistors that is larger than a spacing between the second gate electrode and a second contact hol for connecting a wiring to a source region or a drain region of the second MOS transistors.

To assist the Office in considering the foregoing features of Claim 1, but without any intent to limit th

claim, reference is made to Figures 7(a), 7(b), 8(a), and 8(b) and the corresponding parts of Applicants' specification on pages 17-19. By way of non-limiting example, the first MOS transistors of Claim 1 are represented by the MOS transistor of Fig. 8(a) and the second MOS transistors are represented by the MOS transistor of Fig. 8(b). The MOS transistor of Fig. 8(a) is used for 2.5V specification, for example, but can be used for 3.3V specification by enlarging the gate length as shown in Fig. 7(a), because the spacing between the first gate electrode of the first MOS transistor and the first contact hole is large enough for 3.3V specification as in Fig. 7(a), for example.

Accordingly, this invention can provide a semiconductor device that realizes high-speed operation that conforms to plural supply voltages, compared to Figs. 31-33, in which the first MOS transistors are optimized at 3.3V specification and are used at 2.5V. See page 3, line 6 to page 5, line 8 of Applicants' specification.

Furthermore, the invention provides such a semiconductor device that can realize low production costs compared to the device of Fig. 34 in which two types of first MOS transistors of 2.5V and 3.3V sp cifications are

formed in a semiconductor chip. See Fig. 34, and page 5, line 9 to page 6, line 15 of Applicants' specification.

Independent Claim 2 recites, inter alia, a gate length of a first electrode of a plurality of first MOS transistors that is larger than a gate length of a second gate electrode of a plurality of second MOS transistors, and a spacing between an edge of a first active region in which the first MOS transistors are formed and a first contact hole for connecting a wiring to a source region or a drain region of the first MOS transistors that is larger than the spacing between an edge of a second active region in which the second MOS transistors are formed and a second contact hole for connecting a wiring to a source region or a drain region of the second MOS transistors.

To assist the Office in considering the foregoing features of Claim 2, but without any intent to limit the scope of the claim, reference is made to Fig. 26 and the corresponding part of Applicants' specification on page 30. The first MOS transistors of Claim 2 are represented, for example, by the 2.5V withstanding MOS transistor of Fig. 8(a), and the second MOS transistor by the 1.5V withstanding transistor of Fig. 8(b). The advantages

achieved by the invention recited in Claim 2 are the same as those discussed above with regard to Claim 1.

The features of Claims 1 and 2 specified above are not taught or suggested by Fifield et al., and the deficiencies of Fifield are not cured by Feng, who describes dual gate oxide thicknesses, i.e., a thin gate oxide that might be needed for a low voltage, low power dissipation device and a thick gate oxide that might be needed for a high voltage, high speed, high current drive device built on the same integrated circuit. In Feng, see column 1, lines 11-16, the thin gate transistor 22 and the thick gate transistor of Fig. 5, and column 3, lines 35-37.

In conclusion, it is respectfully submitted that there is no basis for combining the teachings of Feng with the t achings of Fifield et al. in any reasonable manner that would produce the inventions recited in independent Claims 1 and 2, or in claims dependent thereon.

The specification has been amended to correct minor errors. A marked-up copy of the amended paragraphs of the specification and of the amended claims is attached.

This application is now believed to be in condition for allowance.

The Examiner is authorized to cancel non-elected Claims 8-20 in order to pass this application to issue.

The Commissioner is hereby authorized to charge to Deposit Account No. 50-1165 any fees under 37 C.F.R. §§ 1.16 and 1.17 that may be required by this paper and to credit any overpayment to that Account. If any extension of time is required in connection with the filing of this paper and has not been requested separately, such extension is hereby requested.

Respectfully submitted,

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Marked-up Copy of Amended Claims -- Appln. No. 10/002,009:

1. (Amended) A semiconductor device including an input circuit or an output circuit configured with a plurality of first MOS transistors in a first area of a principal plane on a semiconductor substrate, and an internal circuit configured with a plurality of second MOS transistors in a second area of the principal plane on th semiconductor substrate,

wherein a first voltage is applied to said plurality of first MOS transistors,

wherein a second voltage smaller than said first voltage is applied to said plurality of second MOS transistors,

wherein a gate length of a first gate electrode of said plurality of first MOS transistors is larger than a gate length of a second gate electrode of said plurality of second MOS transistors, and

wherein a spacing between said [a] first gate electrode of the first MOS transistors [constituting the input circuit or the output circuit] and a first contact hole for connecting a wiring to a source region or a drain r gion of the first MOS transistors is larger than a

spacing between said second gate electrode and a second contact hole for connecting a wiring to a source region or a drain region of the second MOS transistors [a minimum processing dimension of the spacing between the first gate electrode and the first contact hole, and

wherein a spacing between a second gate electrode of the second MOS transistors constituting the internal circuit and a second contact hole for connecting a wiring to a source region or a drain region of the second MOS transistors is equal to a minimum processing dimension of the spacing between the second gate electrode and the second contact hole].

2. (Amended) A semiconductor device including an input circuit or an output circuit configured with a plurality of first MOS transistors in a first area of a principal plane on a semiconductor substrate, and an internal circuit configured with a plurality of second MOS transistors in a second area of the principal plane on th semiconductor substrate,

wherein a first voltage is applied to said plurality of first MOS transistors,

wherein a second voltage smaller than said first voltage is applied to said plurality of second MOS transistors,

wherein a gate length of a first gate electrode of said plurality of first MOS transistors is larger than a gate length of a second gate electrode of said plurality of second MOS transistors, and

wherein a spacing between an edge of a first active region in which the first MOS transistors [constituting th input circuit or the output circuit] are formed and a first contact hole for connecting a wiring to a source region or a drain region of the first MOS transistors is larger than a spacing between an edge of a second active region in which the second MOS transistors are formed and a second contact hole for connecting a wiring to a source region or a drain region of the second MOS transistors [a minimum processing dimension of the spacing between the edge of th first active region and the first contact hole, and

wherein a spacing between an edge of a second active region in which the second MOS transistors constituting th internal circuit are formed and a second contact hole for connecting a wiring to a source or a drain region of the s cond MOS transistors is qual to a minimum processing

dimension of the spacing between the edge of the second active region and the second contact hole].

3. (Twice Amended) A semiconductor device according to Claim 1,

wherein said input circuit or said output circuit operates with said first voltage, and

wherein said internal circuit operates with said second voltage

[wherein a power supply voltage applied to the first MOS transistors constituting the input circuit or the output circuit is equal to a power supply voltage applied to the second MOS transistors constituting the internal circuit].

4. (Twice Amended) A semiconductor device according to Claim 1 [2],

wherein said plurality of first MOS transistors are first voltage withstanding MOS transistors, and

wherein said plurality of second MOS transistors are second voltage withstanding MOS transistors

[wherein a gate length of the first MOS transistors is equal to a gat l ngth of th second MOS transistors].

5. (Amended) A semiconductor device according to Claim 1 [3],

wherein a gate insulating film thickness of the first MOS transistors is larger than [equal to] a gate insulating film thickness of the second MOS transistors.

6. (Amended) A semiconductor device according to Claim 1 [3],

wherein an area of the active region in which the first MOS transistors are formed is larger than an area of the active region in which the second MOS transistors are formed.

7. (Twice Amended) A semiconductor device according to Claim 1,

wherein said plurality of first MOS transistors are p-channel type, and the source of each of said plurality of first MOS transistors is supplied with said first voltage, and

wherein said plurality of second MOS transistors are p-channel type, and the source of each of said plurality of second MOS transistors is supplied with said second voltage

[wherein a power supply voltage applied to the first MOS transistors constituting the input circuit or the output circuit is higher than a power supply voltage applied to the second MOS transistors constituting the internal circuit].

21. (Amended) A semiconductor device according to Claim 2,

wherein said input circuit or said output circuit operates with said first voltage, and wherein said internal circuit operates with said second voltage

[wherein a power supply voltage applied to the first MOS transistors constituting the input circuit or the output circuit is equal to a power supply voltage applied to the second MOS transistors constituting the internal circuit].

22. (Amended) A semiconductor device according to Claim 2 [21],

wherein said plurality of first MOS transistors are first voltage withstanding MOS transistors, and

wherein said plurality of second MOS transistors are s cond voltag withstanding MOS transistors

[wherein a gate length of the first MOS transistors is equal to a gate length of the second MOS transistors].

23. (Amended) A semiconductor device according to Claim 2 [3],

wherein a gate insulating film thickness of the first MOS transistors is larger than a gate insulating film thickness of the second MOS transistors

[wherein a gate length of the first MOS transistors is equal to a gate length of the second MOS transistors].

24. (Amended) A semiconductor device according to Claim 2 [21],

wherein an area of the active region in which the first MOS transistors are formed is larger than an area of the active region in which the second MOS transistors are formed

[wherein a gate insulating film thickness of the first MOS transistors is equal to a gate insulating film thickness of the second MOS transistors].

25. (Amended) A semiconductor device according to Claim 2 [21],

wherein said plurality of first MOS transistors are p-channel type, and the source of each of said plurality of first MOS transistors is supplied with said first voltage, and

wherein said plurality of second MOS transistors are p-channel type, and the source of each of said plurality of second MOS transistors is supplied with said second voltage [wherein an area of the active region in which the first MOS transistors are formed is larger than an area of the active region in which the second MOS transistors are formed].

with the same function individually by each of the supply voltage specifications will require enormous design works, which invites an elongated development term and increased production cost. Therefore, the usual practice searches for common grounds as much as possible in the specifications of the circuits that can be designed commonly, thus enhancing the design efficiency.

SUMMARY OF THE INVENTION

The inventors has examined the circuit configuration of the LSI that has the same function and conforms to the two types of the external supply voltage specifications. The system that the inventors has examined will be outlined as follows.

Fig. 29 illustrates one example of the supply voltage specifications required for an LSI. The two types of external supply voltages (VDD) to be supplied to the LSI are assumed to be 3.3 V and 2.5 V; and the I/O supply voltages (VDDQ) are assumed to be 3.3 V and 2.5 V. The I/O supply voltages (VDDQ) represent the maximum values of the input signal levels that are inputted to the LSI. The internal supply voltages (VDDI) (supply voltages for the internal circuits) are assumed to be 1.5 V in both specifications.

Fig. 30 illustrates one example of the gate insulating film thickness (TOX) and the minimum processing gate length (Lg)

of the MOS transistor that is optimized so as to conform to the above three kinds of supply voltages (3.3 V, 2.5 V, 1.5 V). As the supply voltage applied to the MOS transistor increases, the gate insulating film thickness (TOX) becomes thicker, and the minimum processing gate length (Lg) becomes longer accordingly.

Fig. 31 illustrates one example of the LSI circuit construction conforming to the supply voltage specifications shown in Fig. 29. The LSI (000) is composed of an input circuit (001), step-down circuit (002), internal circuit (101), and output circuit (003). The step-down circuit (002) lowers the external supply voltage (VDD) to the internal supply voltage (VDDI), which is supplied to the internal circuit (101). The input circuit (001) and the output circuit (003) are directly supplied with the input signal (IN) and the I/O supply voltage (VDDQ) that varies depending upon the external supply voltage specifications.

In the foregoing circuit construction, by designing the step-down circuit (002) to bring the internal supply voltage (VDDI) into 1.5 V in either case of the external supply voltage (VDD) being 3.3 V and 2.5 V, the design and manufacturing process of the internal circuit (101) can be unified into two types of LSIs. That is, in either of the LSIs, the internal circuit (101) is supplied only with the supply voltage of 1.5 V, and the internal circuit can be formed with MOS transistors having the

the input circuit (001) and the output circuit (003), in the LSI with the specification of the external supply voltage (VDD) being 2.5 V. However, in either of the LSI of 2.5 V specification and the LSI of 3.3 V specification, the size of the input/output circuit becomes double, compared with the first circuit construction, which leads to a problem that increases the chip size and the production cost.

The present invention has been made in view of these circumstances, and it is an object of the invention to provide a system that realizes the high-speed operation of a semiconductor device that conforms to plural supply voltage specifications.

Another object of the invention is to provide a system that reduces the production cost of a semiconductor device conforming to plural supply voltage specifications.

Another object of the invention is to provide a system that shortens the development term of a semiconductor device conforming to plural supply voltage specifications.

The above and other objects and novel features of the invention will become apparent from the descriptions and accompanying drawings of this specification.

In accordance with one aspect of the invention, the semiconductor device includes an input circuit or an output circuit configured with a plurality of first MOS transistors

in a first area of a principal plane on a semiconductor substrate, and an internal circuit configured with a plurality of second MOS transistors in a second area of the principal plane on the semiconductor substrate, in which a spacing between a fist gate electrode of the first MOS transistors constituting the input circuit or the output circuit and a first contact hole for connecting a wiring to a source region or a drain region of the first MOS transistors is larger than a minimum processing dimension of the spacing between the first gate electrode and the first contact hole, and a spacing between a second gate electrode of the second MOS transistors constituting the internal circuit and a second contact hole for connecting a wiring to a source region or a drain region of the second MOS transistors is equal to a minimum processing dimension of the spacing between the second gate electrode and the second contact hole.

In accordance with another aspect of the invention, the semiconductor device includes an input circuit or an output circuit configured with a plurality of first MOS transistors in a first area of a principal plane on a semiconductor substrate, and an internal circuit configured with a plurality of second MOS transistors in a second area of the principal plane on the semiconductor substrate, in which a spacing between an edge of a first active region where the first MOS transistors

supply voltage (VDD). Further, the internal circuit 101 is designed to operate with the internal supply voltage (VDDI) of 1.5 V, which is lower than the external supply voltage (VDD), in order for higher speed and lower power consumption.

With regard to the SRAM formed on the first silicon chip 1a and the SRAM formed on the second silicon chip 1b, only part of the MOS transistors constituting the input/output circuit are different, but the other circuits are made up with the same MOS transistors. That is, the SRAM formed on the silicon chip 1a is optimized so that the MOS transistors constituting the input/output circuit can operate at a high speed with the supply voltage of 2.5 V; and the SRAM formed on the silicon chip 1b is optimized so that the MOS transistors constituting the input/output circuit can operate at a high speed with the supply voltage of 3.3 V. These two types of SRAMs are furnished with the step-down circuits that supply the internal circuit 101 with the internal supply voltage (VDDI) of 1.5 V, in either case of 3.3 V and 2.5 V for the external supply voltage (VDD).

Fig. 3 is a concrete circuit diagram of the data output circuit 104, and Fig. 4 is a waveform chart illustrating the internal operations of the data output circuit 104.

Among the MOS transistors that constitute the data output circuit 104, the n-channel MOS transistors (f32, f34, f36) and the p-channel MOS transistors (f31, f33, f35, f37) are directly

supplied with the I/O supply voltage (VDDQ) that differs depending on the external supply voltage specifications. Therefore, the MOS transistors (f31 to f37) formed on the silicon chip 1a are designed to withstand 2.5 V so as to exhibit the high-speed performance when the I/O supply voltage (VDDQ) of 2.5 V is supplied thereto. On the other hand, the MOS transistors (f31 to f37) formed on the silicon chip 1b are designed to withstand 3.3 V so as to exhibit the high-speed performance when the I/O supply voltage (VDDQ) of 3.3 V is supplied thereto. The other MOS transistors of the data output circuit 104 are designed to withstand 3.3 V for both the silicon chip 1a and 1b, so that they can be used with the two kinds of supply voltages (2.5 V, 3.3 V).

Fig. 5 is a concrete circuit diagram of the address input circuit 102 and the data input register 112, and Fig. 6 is a waveform chart illustrating the address input signal AD inputted to the address input circuit 102.

As shown in Fig. 6, usually the address input signal AD is a small amplitude signal appeared against the reference voltage (VREF); however, when it takes the maximum amplitude, the address input signal AD becomes the same voltage as the I/O supply voltage (VDDQ). Therefore, the MOS transistors (f21 and f22) formed on the silicon chip 1a are designed to withstand 2.5 V so as to exhibit the high-speed performance when the I/O

supply voltage (VDDQ) of 2.5 V is supplied thereto. On the other hand, the MOS transistors (f21 and f22) formed on the silicon chip 1b are designed to withstand 3.3 V so as to exhibit the high-speed performance when the I/O supply voltage (VDDQ) of 3.3 V is supplied thereto.

Fig. 7(a) is a plan view of the 3.3 V withstanding MOS transistor formed on the silicon chip 1b, and Fig. 7(b) is a plan view of the 1.5 V withstanding MOS transistor formed on the same silicon chip 1b. The 3.3 V withstanding MOS transistor and the 1.5 V withstanding MOS transistor each have the gate insulating film thickness (TOX) and the minimum processing gate length (Lg) as shown in Fig. 30. In the 3.3 V withstanding MOS transistor, the spacing between the gate electrode 8b and the contact hole 17 for connecting the source and drain regions to the wiring region is formed in the minimum processing dimension (a) of this spacing, in order to promote the microstructure. Also, in the 1.5 V withstanding MOS transistor, the spacing between the gate electrode 8c and the contact hole 16 for connecting the source and drain regions to the wiring region is formed in the minimum processing dimension (a) of this spacing, from the same reason.

Fig. 8(a) is a plan view of the 2.5 V withstanding MOS transistor formed on the silicon chip 1a, and Fig. 8(b) is a plan view of the 1.5 V withstanding MOS transistor formed on

comparison to the minimum processing dimension (a) of this spacing.

Next, as shown in Fig. 21, metal wirings 20 to 27 are formed on the silicon wafer 1A; and, as shown in Fig. 22, metal wirings 20 to 27 are formed on the silicon wafer 1B. The metal wirings 20 to 27 are formed, for example, through the processing of: depositing an aluminum alloy film on the silicon oxide film 15 including the insides of the contact holes 16, 17 by the sputtering method, and patterning the aluminum alloy film by the dry etching with the photo resist film served as the mask. The metal wirings 20 to 27 on the silicon wafer 1A and the metal wirings 20 to 27 on the silicon wafer 1B are formed in the same manner with the same photo mask.

The actual SRAM has the metal wirings of about three layers to overlie the metal wirings 20 to 27, but the detailed explanation will be omitted. These metal wirings are formed by the same system using the same photo mask to the silicon wafer 1A and the silicon wafer 1B, as the metal wirings 20 to 27. Thereafter, the silicon wafer 1A is divided into plural silicon chips 1a, and the silicon wafer 1B is divided into plural silicon chips 1b, thus attaining the silicon chip 1a in which the SRAM of 2.5 V specification is formed, as shown in Fig. 1, and the silicon chip 1b in which the SRAM of 3.3 V specification is formed, as shown in Fig. 2.